

IN THE CLAIMS

This listing of claims replaces all prior listings:

1. (Currently Amended) A nonvolatile magnetic memory device comprising;
 - (a) a transistor for selection, formed in a semiconductor substrate,
 - (b) a first insulating interlayer covering the transistor for selection,
 - (c) a first connecting hole formed in a first opening portion formed through the first insulating interlayer, and connected to the transistor for selection,
 - (d) a first wiring being formed on the first insulating interlayer and extending in a first direction,
 - (e) a second insulating interlayer covering the first insulating interlayer and the first wiring,
 - (f) a tunnel magnetoresistance device being formed on the second insulating interlayer and comprising a tunnel barrier and two ferromagnetic layers, said tunnel barrier being sandwiched between said two ferromagnetic layers, one of the ferromagnetic layers including an anti-ferromagnetic layer and a pinned magnetic layer,
 - (g) a third insulating interlayer covering the tunnel magnetoresistance device and the second insulating interlayer,
 - (h) a second wiring being formed on the third insulating interlayer, being electrically connected to one end of the tunnel magnetoresistance device and extending in a second direction different from the first direction, and
 - (i) a second connecting hole formed in a second opening portion formed through the second insulating interlayer, and connected to the first connecting hole,in which an end face of an extending portion of the anti-ferromagnetic layer but not the pinned magnetic layer ~~other end of the tunnel magnetoresistance device~~ is in contact with the second connecting hole.

2. (Withdrawn) A manufacturing method of a nonvolatile magnetic memory device, comprising the steps of;

- (A) forming a transistor for selection, in a semiconductor substrate,
- (B) forming a first insulating interlayer on the entire surface,
- (C) forming a first opening portion through the first insulating interlayer, and forming a first connecting hole connected to the transistor for selection in the first opening portion,

(D) forming a first wiring extending in a first direction on the first insulating interlayer,

(E) forming a second insulating interlayer on the entire surface,

(F) forming a stacking structure constituted at least of a first ferromagnetic layer, a tunnel barrier and a second ferromagnetic layer on the second insulating interlayer,

(G) forming a second opening portion in those portions of the stacking structure and the second insulating interlayer which portions are positioned above the first connecting hole,

(H) forming an electrically conductive layer on the entire surface including an inside of the second opening portion,

(I) patterning the electrically conductive layer, the second ferromagnetic layer and the tunnel barrier, thereby to obtain a second connecting hole connected to the first connecting hole in the second opening portion,

(J) patterning the first ferromagnetic layer, thereby to obtain a tunnel magnetoresistance device having the tunnel barrier sandwiched between the first and second ferromagnetic layers, and also to obtain an extending portion of the first ferromagnetic layer, said extending portion having an end face being in contact with the second connecting hole,

(K) forming a third insulating interlayer on the entire surface, and

(L) forming a second wiring on the third insulating interlayer, said second wiring being electrically connected to the second ferromagnetic layer and extending in a second direction different from the first direction.

3. (Withdrawn) A manufacturing method of a nonvolatile magnetic memory device, comprising the steps of;

(A) forming a transistor for selection, in a semiconductor substrate,

(B) forming a first insulating interlayer on the entire surface,

(C) forming a first opening portion through the first insulating interlayer, and forming a first connecting hole connected to the transistor for selection in the first opening portion,

(D) forming a first wiring extending in a first direction on the first insulating interlayer,

(E) forming a second insulating interlayer on the entire surface,

(F) forming a stacking structure constituted at least of a first ferromagnetic layer, a tunnel barrier and a second ferromagnetic layer on the second insulating interlayer,

(G) patterning the second ferromagnetic layer and the tunnel barrier,

(H) forming a second opening portion through those portions of the first ferromagnetic layer and the second insulating interlayer which portions are positioned above the first connecting hole,

(I) forming an electrically conductive layer on the entire surface including an inside of the second opening portion,

(J) patterning the electrically conductive layer, thereby to form a second connecting hole connected to the first connecting hole in the second opening portion,

(K) patterning the first ferromagnetic layer, thereby to obtain a tunnel magnetoresistance device having the tunnel barrier sandwiched between the first and second ferromagnetic layers,

(L) forming a third insulating interlayer on the entire surface, and

(M) forming a second wiring on the third insulating interlayer, said second wiring being electrically connected to the second ferromagnetic layer and extending in a second direction different from the first direction.

4. (Withdrawn) The manufacturing method of a nonvolatile magnetic memory device according to claim 3, in which the step (G) is followed by a step in which the first ferromagnetic layer is patterned, thereby to obtain the tunnel magnetoresistance device having the tunnel barrier sandwiched between the first and second ferromagnetic layers, and also to obtain the extending portion of the first ferromagnetic layer,

the second opening portion is formed through those portions of the extending portion of the first ferromagnetic layer and the second insulating interlayer which portions are positioned above the first connecting hole in the above step (H), and

the above step (J) is followed by the step (L) while the above step (K) is omitted.